MITEL SEMICONDUCTOR

CLA90000 SERIES

HIGH DENSITY CMOS GATE ARRAYS

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INTRODUCTION

The CLA90000 family of gate arrays from Mitel Semiconductor consists of 14 fixed-size arrays with the option of building optimized arrays with up to 1.1 million gates. This family offers low-power, mixed voltage capability and a high density silicon architecture. The CLA90000 series is easy to use with and without synthesis tools and comes with design utilities to provide customers with a faster time to market.

FEATURES

- Low power, 0.5µW/MHz/gate at 3V supply (NAND 2 loads)
- High density of 5,425 available gates/mm^2
- 3V and 5V I/O capability on the same device
- 150ps gate delay for 2-input NAND with two loads (5V)
- Accurate delay modelling for gates and tracks with *sign off quality* CAE design libraries for QuickSim II and Verilog-XL
- CAD libraries optimized for synthesis
- Up to 512K available gates and 352 pads with fixed arrays
- Up to 1.1M available gates and 520 pads with optimized arrays
- Double or triple layer metal on a 0.6µm (drawn) process
- Operation from 2.7V to 5.5V
- Methodologies for low clock skew
- Phase locked loop cells, both gate array variant and embedded variant with on-chip filter
- Embedded RAM and ROM
- Expanding range of Mitel SytemBuilder™ soft and hard cells for complex functions including 85C30, 8051, and 8251 devices
- Wide range of packaging options including Ball Grid Arrays
- Commercial and military pad density options

BENEFITS

- Fast Customer Time To Market
  - Direct sign-off on industry standard CAE tools
  - Comprehensive industry-standard design tool flows
  - SystemBuilder™ megacell libraries
  - Worldwide design centre support
  - Reliable prototype and production delivery
  - Two silicon sources
- Cost-effective solutions
  - Optimized silicon architecture for excellent silicon utilization
  - Statistical process control for optimum yield
  - High quality and reliability, manufactured to MIL STD 883 methods and other industry recognized standards

OVERVIEW

The CLA90000 series product has a number of important elements that assist designers.

Ease of design

Ease of design is an important feature of this new product, as shown by the checking and verification utilities built into the Mitel design kits. Accurate simulation is essential for good design, and the Mitel 5^{th} order pin to pin delay model algorithms help ensure first time success. Various design routes and industry-standard systems are available.

Cell Libraries

Cell libraries are optimized for synthesis and include a complete range of soft and hard macros. Cells include basic logic, oscillators, JTAG controllers and macros from the extensive SystemBuilder™ library such as microprocessors, memories, UARTs, and DSP elements, which improve time to market through a shorter design cycle. Embedded custom blocks can be inserted into a gate array to produce dense memory or other compact high performance components. Optimized arrays can offer gate array cycle times if embedded blocks are defined early in the design cycle.

CLA90000 SERIES

Silicon and process

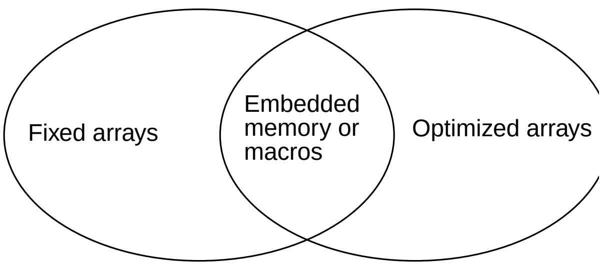
This generation of gate arrays uses a 0.6µm process and meets its primary objectives of dense architecture and low power without compromising performance. Packing density is 5,500 available gates per mm^2, with utilization for three-layer metal typically exceeding 70% (random logic). Power consumption is low with both 5V and 3V supplies, reaching 0.5µW/MHz/gate at 3V with two gate loads.

Service

The service Mitel offers to customers encompasses product guidance from a marketing team, engineering expertise, including design advice and in-depth knowledge of CAE tools, through to fast delivery and world class quality and reliability standards.

ARRAY SIZES

CLA90000 consists of a series of fixed, embedded and optimized arrays that can be combined as shown below.



Standard, fixed array sizes are prefabricated and appropriate probe cards are available for fast turn around and low cost.

For a design with a large memory (2k bits or more) or when an embedded macro like an ARM RISC microprocessor is required, all device layers can be fabricated. An embedded array uses the fixed array bases but with a section of the array removed to make space for the custom block. Optimized arrays are customized to the application, can be built with the required number of pads or gates, and can also include embedded cells.

Optimized arrays are most often used in medium- to high-volume applications where the larger engineering cost is balanced by lower production pricing. For high volume devices, an optimized array can be generated at Mitel using automated tools. The Mitel Design Centres can advise on the best options, in terms of fixed gate arrays and standard cells, for a given design.

Embedded and optimized arrays are as easy to design with as the fixed array bases, and have similar prototyping times provided custom cell definition or new array size is decided early in the design.

A wide range of packages is offered for both the fixed and optimized arrays, and all arrays offer the choice of commercial or military pad density. The lower pad density meets the need of MIL STD customers in terms of bond wire spacing specifications.

CLA90000 has a range of fixed array bases to offer a suitable array size for most applications, from low to high volume.

Fixed Gate Arrays

Array	No. of Gates	Typical Utilization of Gates		Number of Pads	
		2-layer metal	3-layer metal	High	Low#
CLA 901	21632	9700	15000	84	44
CLA 902	32768	14000	23000	100	52
CLA 903	57800	26000	40000	128	64
CLA 904	75272	33000	52000	144	72
CLA 905	95048	42000	66000	160	80
CLA 906	141512	63000	99000	192	96
CLA 907	168200	75000	117000	208	104
CLA 908	228488	102000	160000	240	120
CLA 909	262088	117000	183000	256	128
CLA 910	297992	134000	208000	272	136
CLA 911	336200	151000	235000	288	144
CLA 912	376712	169000	263000	304	152
CLA 913	419528	188000	293000	320	160
CLA 914	512072	230000	358000	352	176

Optimized Gate Arrays

Array	Max. No. of Gates	Typical Utilization of Gates		Max. Number of Pads	
		2-layer metal	3-layer metal	High	Low#
*CLA9XX	114912 8	517000	804000	520	264

* optimized arrays available up to 1.1M gates.

MIL density pad spacing

Choosing an Array

To find the most suitable array for an application, refer to the array table on the left and find the smallest one that has enough pads, remembering to look at the correct pad density column and to include power and ground pads. If the array has enough gates, the design is ‘pad limited’, and will have spare gates. If the design needs more gates, and therefore a bigger array, it is ‘gate limited’ and will have spare pads.

An additional consideration is the number of I/O pins that can be tested by automatic test equipment. The locally based Mitel Design Centre will help resolve any testing issues.

If a design is pad limited, it requires the smallest array with sufficient pads. Two-layer metal (CLA prefix) is generally the most economical. If the selection process arrives at a gate limited design, it requires the smallest array with sufficient usable gates and three-layer metal (CLT prefix) will generally be lower cost. Also, if a special clock or power distribution scheme is required, three layer metal is often needed.

ARCHITECTURE

- Compact routable core cell
- Typical design reduced in silicon area by up to 50% over the previous gate array generation
- Utilization from 45% to 80% for triple-layer metal, depending on design topology
- Efficient register file RAM (3 gates/bit)
- Custom full layer (embedded) RAM option for larger memories

The gate array core cell was chosen after researching a number of different cell layouts. The core cell contains four transistors, two NMOS and two PMOS. These are built as one structure with a shared central source/drain region with the polysilicon gates independently available. This core cell layout gives efficient metal interconnections for a range of logic gates, flip-flops, and register file RAM, and also permits over-cell routing to increase gate utilization.

I/O ARRANGEMENT

- I/O cell options for 3V and 5V supply
- 3V and 5V I/O on the same device
- Slew rate control on outputs
- Excellent ESD protection to 3kV and good latch-up immunity to 200mA, meets STACK 0001 V12.1 and MIL STD 883
- PCI /PC Card fully compatible I/Os

A wide range of I/O cells is available, and each one has three forms to suit 3V, 5V, or mixed 3 and 5V operation. Also, each I/O cell can be individually configured as one of the following:

- Input
- Output
- Tristate output
- Open drain output
- Open source output
- Bidirectional
- Open drain bidirectional
- Open source bidirectional

The I/O stage has a number of components used to construct a wide variety of I/O cells, including pullup and pulldown resistors and small transistors for oscillators. 5V cells are available with TTL or CMOS compatible input Schmitt circuitry. 3V cells meet both TTL and CMOS specifications.

The CLA90000 has four separate internal supply rails: one for the core, one for the buffer, and two for output areas of the chip. The buffer supply rail is completely isolated for very low noise. This offers the benefit of good noise immunity with multiple supply voltage capability to suit the application. The mixed 3 and 5V I/O capability can be used for power saving or interfacing with 3V and 5V systems.

Slew rate control is provided within the I/O output drive circuitry to minimize switching noise transients. This is a useful feature in larger designs, particularly where multiple high drive outputs switch simultaneously. It also reduces reflections from unterminated pc board tracks.

Electrostatic discharge (ESD) protection is built into the input and output cells, and has been designed to withstand in excess of 3kV (human body model). The structure and process is also highly resistant to latch-up and able to withstand forward bias currents in excess of 200mA.

CLOCK AND POWER DISTRIBUTION

- Low clock skew distribution strategies
- Power grid to minimize voltage drop

It is known in the industry that large, complex designs working at high speed are vulnerable to problems associated with poor clock and power distribution. The following sections indicate how the Mitel design and layout methodology avoids these problems.

Clock Distribution

Mitel has experience with a variety of layout methods to prevent clock skew problems. The preferred method is to use built-in clock grid generation and drive the clock grids with buffers distributed throughout the chip, which limits skew to below 70ps and provides a reliable solution to clock distribution suitable for most designs. For all clock strategies, post-layout clock delays are extracted and fed back for resimulation. An example of one clock distribution method is illustrated below.

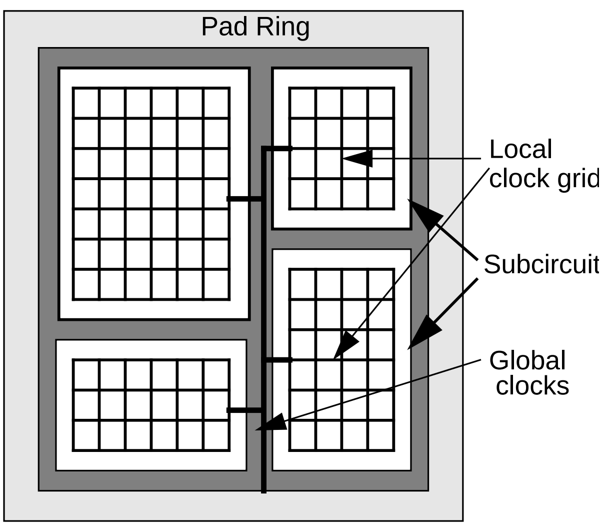


Figure 1 Example Clock Distribution

Power Distribution and Estimation

The Mitel layout methodology constructs grids for all array size options, including optimized arrays. This grid can use metal layers one and two for horizontal and vertical grids, and metal layer three may also be used on some larger arrays. Methods of implementation are available for use with flat layout, manual methods, or hierarchy. A simplified grid arrangement is shown below. In addition the CLA90000 series of arrays is supported by EPIC PowerMill™ power estimation software (check availability)..

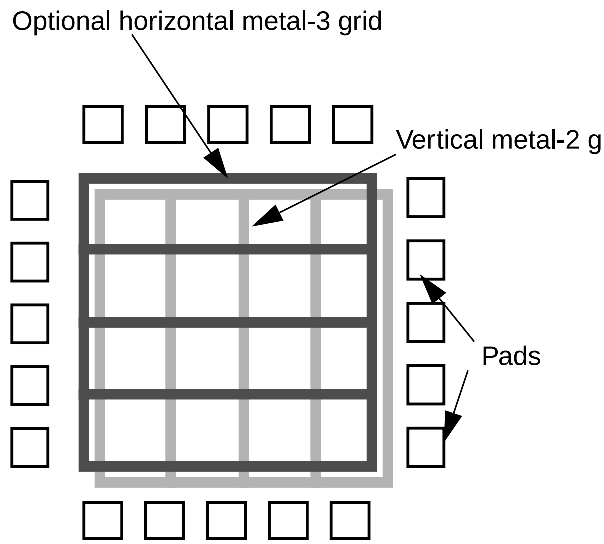


Figure 2 Power Grid

MANUFACTURING

- Class 10 clean room
- Advanced equipment including mini-environments and SMIF box transportation between processes
- Statistical process control (SPC) monitoring of all stages
- Vibration-free for reliable manufacture
- Two silicon sources

The CLA90000 product is manufactured near Plymouth, England in a purpose-built vibration-free factory for submicron process geometries. The factory uses the latest automated equipment for 8-inch wafers in class 10 clean room conditions with SMIF boxes for semi-automatic handling. Computer aided manufacture ensures production efficiency and the lowest possible defect level. In addition to the world class wafer fabrication facility, the probe and final test areas are equipped with the latest analog and digital testers. Mitel Semiconductor is committed to continuous investment to provide state-of-the-art CMOS ASICs. A qualified second source for this silicon process is available.

DESIGN SUPPORT

- Flexible design routes
- Proven right first time design
- Local design support

Design and layout support for the CLA90000 arrays is available from many local centres worldwide, each connected to our headquarters via high speed data links. A design centre engineer, as part of the Mitel support team, is assigned to each customer circuit to give full assistance with all aspects of the design and to ensure a smooth and efficient design flow.

Mitel offers both customer and turnkey design routes, to allow for varying types of customer interface while maintaining our responsibility to ensure first time working devices.

The design process incorporates a design audit procedure to verify compliance with customer specification and to ensure manufacturability. The procedure includes three review meetings with the customer held at key stages of the design. This is illustrated in the diagram on the next page.

Design review one:	Held at the beginning of the design cycle to check and agree on performance, packaging, specifications and design timescales.
Design review two:	Held after logic simulation but prior to layout to ensure satisfactory functionality, timing performance, and adequate fault coverage.
Design review three:	Held after layout and post-layout simulation verification of satisfactory design performance after insertion of actual track loads. Final check of all device specifications before prototype manufacture.

CAE Support

- Synthesis with Synopsys, Mentor or Cadence
- Sign-off simulation with Mentor or Cadence
- VIEWlogic VCS simulator supported
- VITAL compliant library
- Full top-down design flow support
- Point tools supported, including Zycad and Powermill
- Direct route to layout and test
- Advanced delay modelling and netlist checking

It is Mitel policy to fully support industry-standard CAE systems that enable a customer to sign off their design without resimulation on a golden simulator. This has the benefit to the customer of not having to learn new tools, and to use the tools they prefer and are familiar with. There is no overhead in engineering effort or time taken rechecking simulation results.

Mitel offers libraries for synthesis tools such as Synopsys, Mentor Autologic II, and Cadence Synergy. This allows a full hierarchical or top-down approach to logic design. The Mitel Universal Delay Compiler (UDC) is supplied with all design kits for advanced delay modelling and comprehensive netlist checking. The UDC matches Synopsys and Mentor native delay calculation.

The advanced features of the synthesis and simulation tools are used for nonlinear delay modelling for better simulation accuracy. This is implemented for optimum speed depending on the particular tool. Other advanced features are supported where they are available.

The information supplied by the customer in the approved CAE vendor format is used as a direct input to the tools that perform the layout and generate the test program.

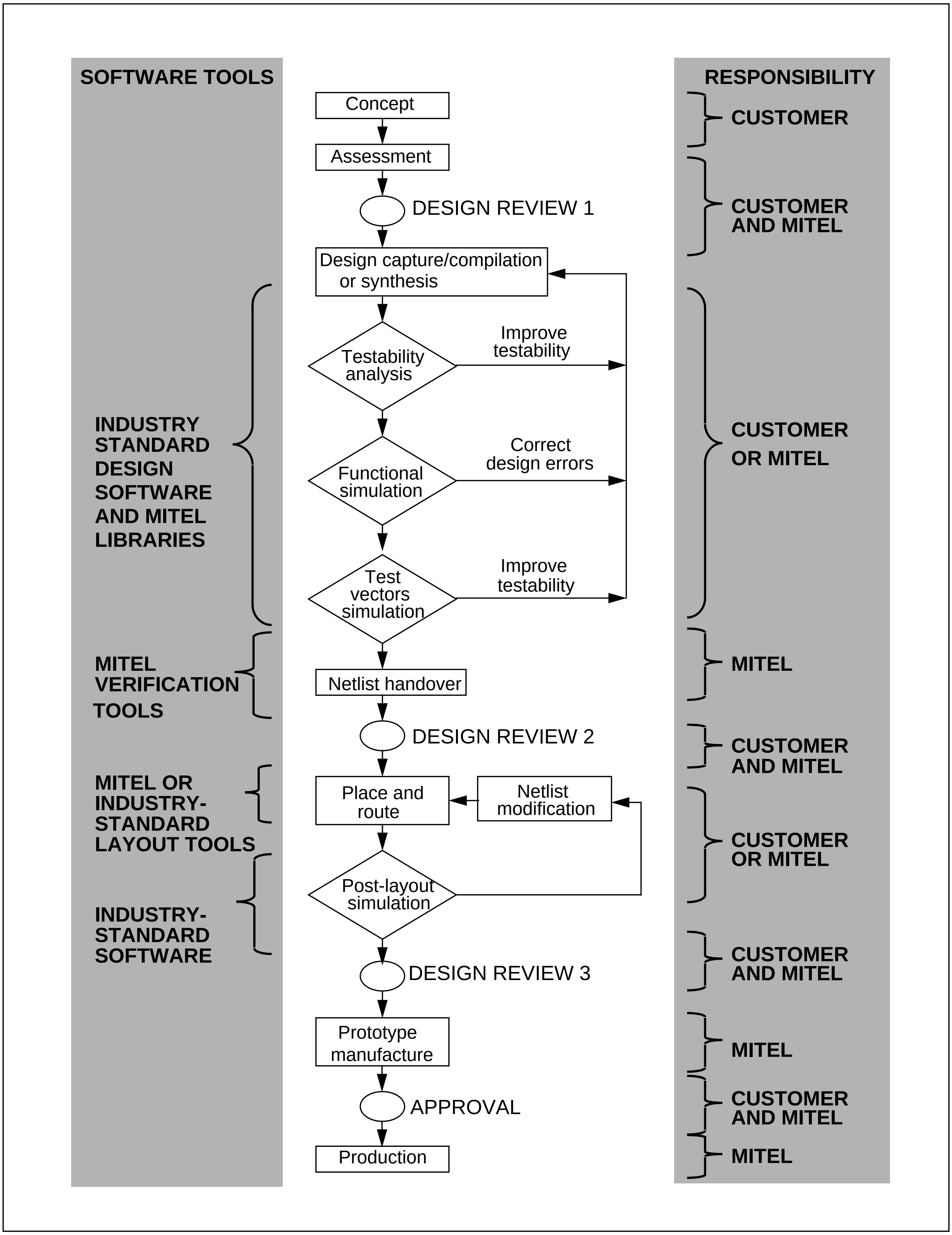


Figure 3 Design Flow

ADVANCED DELAY MODELLING

- Edge speed modelling
- Pin to pin timings
- Nonlinear delay modelling
- Accurate delay derating

Pin to Pin Delays

Delay models use times between individual input and output pins for both rising and falling delays, as illustrated below.

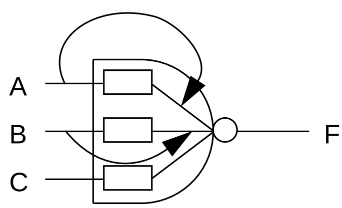


Figure 4 Delay Paths

The use of individual pin to pin delays, e.g. A to F and B to F, improves simulation accuracy as there can be considerable variation in delay between different input pins. For complex gates (e.g. AND-NOR gates or adders) the variation is up to 40%. For simple NAND and NOR logic gates the typical variation is 20%.

Nonlinear Curve Fitting

For fast input edges (0.5ns) delay time increases linearly with the output load, whereas for high output loads delay increases linearly with edge speed. Delays for slow input edges and light input loads do not follow the linear model, so a simple linear model cannot represent delays accurately. A more complex formula, which includes interaction between edge and load factors, is used to model delays for CLA90000.

THERMAL MANAGEMENT

- Lower power CMOS for improved thermal management
- 0.5µW/MHz/gate (3V supply 2-input NAND with 2 loads)
- Software constructed power grids for efficient power distribution
- Copper lead frame QFPs for lower thermal resistance
- High pinout power packages available

The increase in speed and density available through advanced CMOS processes results in a corresponding increase in power dissipation. Semicustom designers now have the ability to design circuits in excess of half a million usable gates, and chip power consumption is an important issue.

To meet the requirements of high speed, high gate count designs, Mitel CLA90000 arrays offer low power factors and a selection of power packages for improved thermal management.

QUALITY AND RELIABILITY

- Statistical process control used in manufacture
- Regular sample screening and reliability testing
- Screening to MIL and other recognized standards is available

At Mitel, quality and reliability are built into the product by statistical control of all processing operations and by minimizing random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures with recording of batch by batch data using computerized WIP tracking systems.

A common information management system is used to monitor the manufacturing of Mitel CMOS processes and operations. All products benefit from the use of this integrated monitoring system resulting in the highest quality standards for all technologies.

Further information and reliability results are contained in the Quality MOS Brochure, available from Mitel Sales Offices.

DERATING FOR VOLTAGE PROCESS AND TEMPERATURE

The following figures show how gate delay increases as supply voltage is reduced.

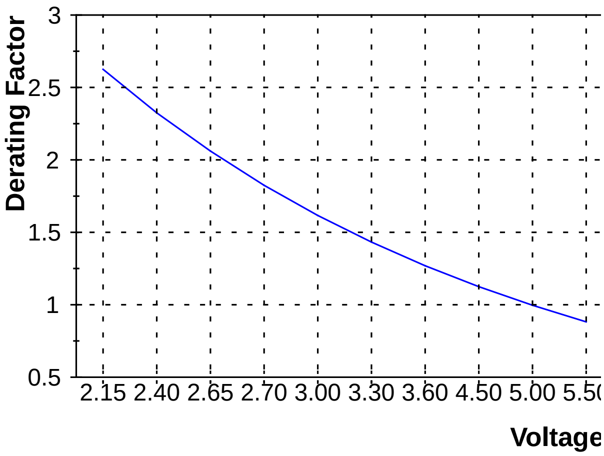


Figure 5 Derating for a 5V supply (5V normalised to 1)

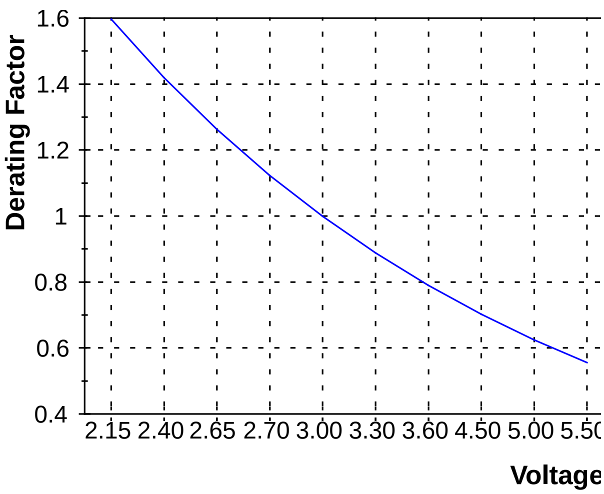


Figure 6 Derating for a 3V supply (3V normalised to 1)

Process Derating

Speed	Derating Factor
slow	1.58
typical	1.00
fast	0.62

Temperature Derating

Note that it is important to use the junction and not the ambient temperature for worst-case simulations.

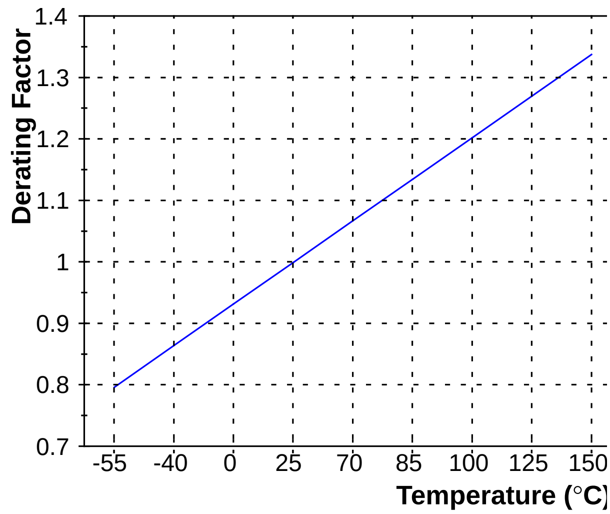


Figure 7 Temperature Derating

AC ELECTRICAL CHARACTERISTICS

For the CLA90000 series, one load unit (LU) is 17fF.

Typical Microcell Delays (ns) (25°C, 0.2ns input edge)

Gates		3V		5V	
		34 fF (2LU)	**68 fF (4LU)**	**34 fF (2LU)**	**68 fF (4LU)**
INVX1	tpLH	0.24	0.34	0.16	0.23
	tpHL	0.12	0.17	0.09	0.11
NAND2X2	tpLH	0.18	0.23	0.13	0.16
	tpHL	0.15	0.19	0.10	0.12
NOR2x2	tpLH	0.31	0.41	0.20	0.26
	tpHL	0.10	0.13	0.07	0.09
SDF	tpLH	0.81	0.91	0.49	0.55
	tpHL	0.61	0.67	0.37	0.41

Typical I/O Delays (25°C, 0.2ns input edge)

I/O delays depend on the voltage of the device, i.e. all 5V I/O, all 3V I/O, or mixed 3V and 5V I/O. The tables below give example delays for each of these cases.

Example delays for 3V only I/O (ns)

Outputs			
		50pF	**100pF**
6mA bistate	tpLH	4.16	6.20
	tpHL	4.72	5.66
		100 pF	**200 pF**
12mA bistate	tpLH	4.26	6.30
	tpHL	4.75	5.68

Inputs		
	34fF (2 LU)	**68fF (4 LU)**
tpLH	0.88	0.93
tpHL	1.29	1.31

Example delays for 5V only I/O (ns)

Outputs			
		50pF	**100pF**
12mA bistate	tpLH	2.87	4.11
	tpHL	3.58	4.22
		100pF	**200pF**
24mA bistate	tpLH	2.93	4.17
	tpHL	3.61	4.26

Inputs		
	34fF (2 LU)	**68fF (4 LU)**
tpLH	0.45	0.48
tpHL	0.70	0.72

Example delays for mixed 3V and 5V I/O (ns)

Delays for mixed 3 and 5V I/O are not the same as for single voltage designs because of level shifting stages.

3V I/O in a mixed 3V and 5V I/O design

Outputs			
		50pF	**100pF**
6mA bistate	tpLH	4.16	6.20
	tpHL	4.72	5.66
		100pF	**200pF**
12mA bistate	tpLH	4.25	6.29
	tpHL	4.75	5.68

Inputs		
	68fF	**136fF**
tpLH	0.79	0.82
tpHL	0.82	0.86

5V I/O in a mixed 3V and 5V I/O design.

Outputs			
		50pF	**100pF**
12mA bistate	tpLH	4.01	5.25
	tpHL	3.68	4.33
		100pF	**200pF**
24mA bistate	tpLH	4.14	5.38
	tpHL	3.74	4.39

Inputs		
	34fF	**68fF**
tpLH	0.45	0.48
tpHL	0.70	0.72

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage	-0.5	7.0	V
Input voltage	-0.5	V_{DD}+0.5	V
Output voltage	-0.5	V_{DD}+0.5	V
Static discharge voltage (HBM)		4	kV
Storage temperature			
Ceramic	-65	150	°C
Plastic	-55	150	°C

Exceeding the absolute maximum ratings may cause permanent damage to the device. Extended exposure at the maximum ratings will affect device reliability.

HBM stands for Human Body Model.

Normal Operating Conditions

Parameter	Min.	Max.	Units
Supply voltage	2.7	5.5	V
Input voltage	V_{SS}	V_{DD}	V
Output voltage	V_{SS}	V_{DD}	V
Current per pad		100	mA
Junction temperature			
Ceramic package	-55	+150	°C
Plastic package	-55	+125	°C
Ambient temperature			
Commercial grade	0	70	°C
Industrial grade	-40	85	°C
Military grade	-55	125	°C

Neither performance nor reliability is guaranteed outside these limits. Extended operation above these limits may affect device reliability.

Input Switching Thresholds

All characteristics are for temperatures between -55 and 150°C (junction temperature).

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
CMOS Schmitt - CS						$4.5 \leq V_{DD} \leq 5.5V$
Input low voltage	V_{IL}			$0.2V_{DD}$	V	
Input high voltage	V_{IH}	$0.7V_{DD}$			V	
Hysteresis	V_H	400			mV	
TTL Schmitt - TS						$4.5 \leq V_{DD} \leq 5.5V$
Input low voltage	V_{IL}			0.8	V	
Input high voltage	V_{IH}	2.0			V	
Hysteresis	V_H	300			mV	
Low voltage Schmitt - BS/NS						$2.7 \leq V_{DD} \leq 3.3V$
Input low voltage	V_{IL}			$0.2V_{DD}$	V	
Input high voltage	V_{IH}	2.0			V	
Hysteresis	V_H	300			mV	
Low voltage Schmitt - BS/NS						3.0 £ VDD £ 3.6V
Input low voltage	V_{IL}			0.2VDD	V	
Input high voltage	V_{IH}	2.2			V	
Hysteresis	V_H	100			mV	

Note: CS cells are 5V CMOS compatible, TS cells are 5V TTL compatible and all other cells are 3V compatible.

Output Voltages and Currents

All characteristics are for temperatures between -55 and 150°C (junction temperature).

Characteristic	Symbol		Value		Unit	Conditions
		Min.	Typ.	Max.		
High output voltage						$2.7 \le V_{DD} \le 3.6V$
All outputs	V_{OH}		V_{DD}-0.05		V	I_{OH} = -1µA
01N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -0.5mA
02N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -1mA
03N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -1.5mA
06N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -3mA
12N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -6mA
Low output voltage						$2.7 \le V_{DD} \le 3.6V$
All outputs	V_{OL}		V_{SS}+0.05		V	I_{OL} = 1µA
01N	V_{OL}		0.2	0.4	V	I_{OL} = 1mA
02N	V_{OL}		0.2	0.4	V	I_{OL} = 2mA
03N	V_{OL}		0.2	0.4	V	I_{OL} = 3mA
06N	V_{OL}		0.2	0.4	V	I_{OL} = 6mA
12N	V_{OL}		0.2	0.4	V	I_{OL} = 12mA
High output voltage						$4.5 \le V_{DD} \le 5.5V$
All outputs	V_{OH}		V_{DD}-0.05		V	I_{OH} = -1µA
01N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -2mA
02N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -4mA
03N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -6mA
06N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -12mA
12N	V_{OH}	0.8V_{DD}	0.9V_{DD}		V	I_{OH} = -24mA
Low output voltage						$4.5 \le V_{DD} \le 5.5V$
All outputs	V_{OL}		V_{SS}+0.05		V	I_{OL} = 1µA
01N	V_{OL}		0.2	0.4	V	I_{OL} = 2mA
02N	V_{OL}		0.2	0.4	V	I_{OL} = 4mA
03N	V_{OL}		0.2	0.4	V	I_{OL} = 6mA
06N	V_{OL}		0.2	0.4	V	I_{OL} = 12mA
12N	V_{OL}		0.2	0.4	V	I_{OL} = 24mA

Short Circuit Currents

All characteristics are for temperatures between -55 and 150°C (junction temperature).

Characteristic	Symbol		Value		Unit	Conditions
		Min.	Typ.	Max.		
Output short circuit current						V_{DD} = 5.5V
01N	I_{OS}	20		60	mA	$V_O = V_{DD}$
02N	I_{OS}	40		120	mA	
03N	I_{OS}	50		160	mA	
06N	I_{OS}	100		300	mA	
12N	I_{OS}	190		560	mA	
Output short circuit current						V_{DD} = 5.5V
01N	I_{OS}	-10		-36	mA	$V_O = V_{SS}$
02N	I_{OS}	-20		-70	mA	
03N	I_{OS}	-30		-100	mA	
06N	I_{OS}	-55		-190	mA	
12N	I_{OS}	-100		-340	mA	
Output short circuit current						V_{DD} = 3.6V
01N	I_{OS}	8		35	mA	$V_O = V_{DD}$
02N	I_{OS}	16		70	mA	
03N	I_{OS}	20		100	mA	
06N	I_{OS}	40		185	mA	
12N	I_{OS}	80		350	mA	
Output short circuit current						V_{DD} = 3.6V
01N	I_{OS}	-3		-20	mA	$V_O = V_{SS}$
02N	I_{OS}	-6		-35	mA	
03N	I_{OS}	-9		-55	mA	
06N	I_{OS}	-18		-95	mA	
12N	I_{OS}	-36		-190	mA	

Operating Power

All characteristics are for temperatures between -55 and 150°C (junction temperature).

V_{DD}	Operating Power (P_{DD})
3V	0.5 µW/MHz (note 1)
5V	1.3 µW/MHz (note 1)

Note 1: For NAND2 with two standard loads.

CELL LIBRARY

- Comprehensive range of microcells
- Extensive SystemBuilder™ library of complex functions
- Software generated gate array RAM and high performance embedded RAM and ROM
- Phase locked loop cells, both gate array variant and embedded variant with on-chip filter
- Oscillator cells
- 3.3V and 5V PCI/PC Card cells
- JTAG controller (check availability)

A comprehensive cell library is available for the CLA90000 series including cells for specific applications.

The library is being continually expanded, so please check with your local Mitel representative for the latest additions.

Mitel design kits feature a simple and powerful software tool called the paracell model generator (PMG) that can generate both gate array and embedded RAM. The design route is the same for both RAM types but the cost is different because an embedded RAM requires fabrication of all device layers.

Register File RAM

Gate array RAM is available as either single or dual port RAM with a minimum size of 8 words x 2 bits and a maximum of 256 words x 64 bits. Memory speeds and number of gates uses are summarized in the table below for a typical single-port RAM operating at 5V, 25°C.

Size	Read Access (ns)	Write Cycle (ns)	Size	
			gates	mm^2
24 words x 4 bits	2.60	3.21	696	0.128
256 words x 8bits	11.48	6.31	9918	1.828
256 words x 64bits	12.20	11.22	53766	9.910

Gate Array ROM

Gate array ROM can be from 8 to 64 kbits with a word length of from 2 to 64 bits in steps of 1 bit. The table below shows memory sizes and typical access times for a ROM operatiing at 5V, 25°C.

Size	Read Access (ns)	Size	
		gates	mm^2
24 words x 4 bits	2.61	196	0.04
256 words x 8bits	3.40	1440	0.27
256 words x 64bits	4.24	5472	1.01

Embedded RAM and ROM

Embedded RAM and ROM meet requirements for high density and high performance. Word length can be from 4 to 64 bits and maximum memory size is 64 kbits for RAM and 128 kbits for ROM. The table below is for a typical embedded RAM operating at 5V, 25°C.

Size	Read Access (ns)	Write Cycle (ns)	Size (mm^2)
24 words x 4 bits	3.3	3.7	0.111
256 words x 8 bits	3.4	3.9	0.423
256 words x 64 bits	4.0	4.7	2.059
8192 words x 8 bits	4.2	5.8	5.983

The table below is for a typical embedded ROM operating at 5V, 25°C.

Size	Read Access (ns)	Read Cycle (ns)	Size (mm^2)
256 words x 8 bits	8.6	11.1	0.215
256 words x 64 bits	11.3	14.9	0.827
4096 words x 16bits	14.8	18.1	1.638

SystemBuilder™ Cells

Name	Function	Approx. No. of Gates
M85C30	Two channel enhanced Serial Communications Controller (SCC) with FIFOs	18100
M82530	Two channel enhanced Serial Communications Controller (SCC)	13400
MFDC	High performance PC-compatible floppy disk controller (82077SL) with M765A core	11500
M765A	Extended features floppy disk controller core for FM and MFM formats	10200
M8051	High performance industry-compatible 8-bit microcontroller, 2 timers, serial I/O	*8700
M8237A	General purpose programmable four channel DMA Controller	4100
M8042	8-bit peripheral interface microcontroller with timer (slave microcontroller)	*3700
M8048	Compact embedded industry-compatible 8-bit microcontroller with timer	*3700
M8254	Extended feature three channel Programmable Interval Timer (PIT)	3600
M8253	General purpose three channel Programmable Interval Timer (PIT)	3100
M6845	General purpose programmable CRT Controller	2900
M8251A	Universal Synchronous/Asynchronous Receiver/ Transmitter (USART)	2400
M16C450	Universal Synchronous/Asynchronous Receiver/ Transmitter (UART) (PC-compatible)	2200
M146818	Ultra low power real-time clock with up to 114 bytes of RAM	*2200
M8250B	Universal Asynchronous Receiver/ Transmitter (UART) (PC-compatible)	2200
M8259A	Eight channel cascadable Programmable Interrupt Controller (PIC)	1800
M8490	SCSI for 5380 compatible asynchronous SCSI interfacing	1600
M91C360	High margin floppy and tape data separator for data rates up to 1.25Mbit/s	1400
M8255	General purpose Programmable Peripheral Interface (PPI)	1200
M91C36	High margin floppy disk data separator for data rates up to 1.25Mbit/s	1200
M8868A	Compact UART with configurable data formats	840
M6402	Compact UART with configurable data formats	830
M8288	Bus controller for 8086 and 8088 microprocessors	270
M82288	Bus controller for 80286 microprocessors	230
M82289	Bus arbiter for 80286 microprocessors, supports IEEE-796	200
M82C84A	Clock generator and ready I/F for 8086 and 8088 microprocessors	70
M82C284	Clock generator and ready I/F for 80286 microprocessors	70
MxADD	Fast adder set for 8, 16 and 32 bit DSP functions	140, 260 and 520
MxMPY	Multiplier set for 8x8, 16x16 and 32x32 bit DSP functions	880, 3700 and 14300
MxBRL	Barrel shifter set for 8, 16 and 32 bit DSP functions	80, 170 and 420
MxCOMP	Comparator set for 4, 8, 16 and 32 bit DSP functions	60, 100, 200 and 350

*Excluding RAM and ROM.

AND Gates

Cell Name	Cell Function
AND2	2-input AND x1drive
AND2X2	2-input AND x 2drive
AND2X4	2-input AND x4 drive
AND3	3-input AND x1 drive
AND3X2	3-input AND x2 drive
AND3X4	3-input AND x4 drive
AND4	4-input AND x1 drive
AND4X2	4-input AND x2 drive
AND4X4	4-input AND x4 drive
AND5	5-input AND x1 drive
AND5X2	5-input AND x2 drive
AND6	6-input AND x1 drive
AND6X2	6-input AND x2 drive
AND8	8-input AND x1 drive
AND8X2	8-input AND x2 drive

OR Gates

Cell Name	Cell Function
OR2	2-input OR x1 drive
OR2X2	2-input OR x2 drive
OR2X4	2-input OR x4 drive
OR3	3-input OR x1 drive
OR3X2	3-input OR x2 drive
OR3X4	3-input OR x4 drive
OR4	4-input OR x1 drive
OR4X2	4-input OR x2 drive
OR4X4	4-input OR x4 drive
OR5	5-input OR x1 drive
OR5X2	5-input OR x2 drive
OR6	6-input OR x1 drive
OR6X2	6-input OR x2 drive
OR8	8-input OR x1 drive
OR8X2	8-input OR x2 drive

NAND Gates

Cell Name	Cell Function
NAND2	2-input NAND x1 drive
NAND2X2	2-input NAND x2 drive
NAND2X4	2-input NAND x4 drive
NAND3	3-input NAND x1 drive
NAND3X2	3-input NAND x2 drive
NAND4	4-input NAND x1 drive
NAND4X2	4-input NAND x2 drive
NAND5	5-input NAND x1 drive
NAND5X2	5-input NAND x2 drive
NAND6	6-input NAND x1 drive
NAND6X2	6-input NAND x2 drive
NAND8	8-input NAND x1 drive
NAND8X2	8-input NAND x2 drive

NOR Gates

Cell Name	Cell Function
NOR2	2-input NOR x1 drive
NOR2X2	2-input NOR x2 drive
NOR2X4	2-input NOR x4 drive
NOR3	3-input NOR x1 drive
NOR3X2	3-input NOR x2 drive
NOR4	4-input NOR x1 drive
NOR4X2	4-input NOR x2 drive
NOR5	5-input NOR x1 drive
NOR5X2	5-input NOR x2 drive
NOR6	6-input NOR x1 drive
NOR6X2	6-input NOR x2 drive
NOR8	8-input NOR x1 drive
NOR8X2	8-input NOR x2 drive

AND-OR-INVERTER Gates

Cell Name	Cell Function
A2DO2I	2-2 AOI x1 drive
A2DO2IX2	2-2 AOI x2 drive
A2O2I	2-1 AOI x1 drive
A2O2IX2	2-1 AOI x2 drive
A2O3I	2-1-1 AOI x1 drive
A2O3IX2	2-1-1 AOI x2 drive
A2DO3I	2-2-1 AOI x1 drive
A2DO3IX2	2-2-1 AOI x2 drive
A3O2I	3-1 AOI x1 drive
A3O2IX2	3-1 AOI x2 drive
A3DO2I	3-3 AOI x1 drive
A3DO2IX2	3-3 AOI x2 drive
A2TO3I	2-2-2 AOI x1 drive
A2TO3IX2	2-2-2 AOI x2 drive
AOAI	AOAI x1 drive
AOAIX2	AOAI x2 drive

OR-AND-INVERTER Gates

Cell Name	Cell Function
O2DA2I	2-2 OAI x1 drive
O2DA2IX2	2-2 OAI x2 drive
O2A2I	2-1 OAI x1 drive
O2A2IX2	2-1 OAI x2 drive
O2A3I	2-1-1 OAI x1 drive
O2A3IX2	2-1-1 OAI x2 drive
O2DA3I	2-2-1 OAI x1 drive
O2DA3IX2	2-2-1 OAI x2 drive
O3A2I	3-1 OAI x1 drive
O3A2IX2	3-1 OAI x2 drive
O3DA2I	3-3 OAI x1 drive
O3DA2IX2	3-3 OAI x2 drive
O2TA3I	2-2-2 OAI x1 drive
O2TA3IX2	2-2-2 OAI x2 drive
OAOI	OAOI x1 drive
OAOIX2	OAOI x2 drive

Exclusive OR and Adder Cells

Cell Name	Cell Function
EXNOR	Exclusive NOR x1 drive
EXNORX2	Exclusive NOR x2 drive
EXOR	Exclusive OR x1 drive
EXORX2	Exclusive OR x2 drive
EXNOR3	3-input Exclusive NOR x1 drive
EXNOR3X2	3-input Exclusive NOR x2 drive
EXOR3	3-input Exclusive OR x1 drive
EXOR3X2	3-input Exclusive OR x2 drive
FADD	Full adder x1 drive
FADDX2	Full Adder x2 drive
FADD2	2 bit Full adder x1 drive
FADD2X2	2 bit Full adder x2 drive
HADD	Half adder x1 drive
HADDX2	Half adder x2 drive
INCR	Increment x1 drive
DECR	Decrement x1 drive

Noninverting Buffers

Cell Name	Cell Function
BUFX1	Noninverting buffer x1 drive
BUFX3	Noninverting buffer x3 drive
BUFX7	Noninverting buffer x7 drive

Inverting Buffers

Cell Name	Cell Function
INVX1	Inverting buffer x1 drive
INVX2	Inverting buffer x2 drive
INVX4	Inverting buffer x4 drive
INVX6	Inverting buffer x6 drive
INVX8	Inverting buffer x8 drive

Tristate Buffers

Cell Name	Cell Function
BDRX1	Tristate noninv buffer active low enable x1 drive
BDRX2	Tristate noninv buffer active low enable x2 drive
BDRX4	Tristate noninv buffer active low enable x4 drive
BDRX8	Tristate noninv buffer active low enable x8 drive

Multiplexers

Cell Name	Cell Function
MUX2T1	2-1 MUX non-inverting x1 drive
MUX2T1X2	2-1 MUX non-inverting x2 drive
MUX4T1	4-1 MUX non-inverting x1 drive
MUX4T1X2	4-1 MUX non-inverting x2 drive
MUX8T1	8-1 MUX non-inverting x1 drive
MUX8T1X2	8-1 MUX non-inverting x2 drive

D-type Flip-Flops

Cell Name	Cell Function
SDF	DFF x1 drive
SDFS	DFF with SET x1 drive
SDFR	DFF with CLEAR x1 drive
SDFRS	DFF with SET and CLEAR x1 drive
SMDF	MUX DFF x1 drive
SMDFS	MUX DFF with SET x1 drive
SMDFR	MUX DFF with CLEAR x1 drive
SMDFRS	MUX DFF with SET and CLEAR x1 drive

Transparent Latches

Cell Name	Cell Function
SDL	D latch active high enable x1
SDLR	D latch with clear active high enable x1
SMDL	Mux D latch active high enable x1
BDL	Buffered data latch
BDLR	Buffered data latch with reset
BMDL	MUX buffered D latch, active high enable
SRLATCH	Set reset latch

Special Cells

Cell Name	Cell Function
DELAY	Delay cell
BHOLD	Bus hold
OSC32K	32kHz crystal oscillator
OSCMID	1MHz to 10MHz crystal oscillator
OSCHIGH	10MHz to 16MHz crystal oscillator
OSCVHIGH	16MHz to 25MHz crystal oscillator

Phase Locked Loop Cells

Cell Name	Cell Function
PLLC1M	Gate array phase locked loop
PLLC2M	Embedded phase locked loop with on-chip filter

Memory Paracells

Cell Name	Cell Function
SPRF	Single port register file memory
DPRF	Dual port register file memory
MPRA	Embedded single port RAM
MPDA	Embedded dual port RAM
MPRO	Embedded ROM
HDRO	Gate array ROM

PCI/PC Card Cells

Cell Name	Cell Function
PCIIO1	5V/3.3V I/O cell for 5V or mixed voltage device
PCIIO2	3V I/O cell for 3V device
PCICLK	5V clock buffer for 5V or mixed voltage device
DNPCIIO1	3V I/O cell for mixed voltage device
DNPCICLK	3V clock buffer for mixed voltage device

I/O Cells

Cell Name	5V Core and 5V I/O
ATSIrddN	5V I/O, Schmitt input (TTL)
ACSIrddN	5V I/O, Schmitt input (CMOS)

Cell Name	3V core and 3V I/O
BBSIrddN	3V I/O, Schmitt input (TTL/CMOS)

Cell Name	3V core with 3V and 5V I/O
DTSIrddN	5V I/O, Schmitt input (TTL)
DCSIrddN	5V I/O, Schmitt input (CMOS)
DBSIrddN	3V I/O, Schmitt input (TTL/CMOS, low noise)
DNSIrddN	3V I/O, Schmitt input (TTL/CMOS, low power)

S means Schmitt input, I means inverting input. Each cell has three variations of resistor connection and five drive strength options as follows:
Pullup, pulldown, or no resistor indicated by r=U, D, or N.
Drive strength options indicated by dd=01, 02, 03, 06 or 12.
The final N in the name means noninverting output. The cells can be used at other than 3 or 5 volts, but thresholds may then be out of specification.

I/O Cells

As the tables above show, the cell library contains an extensive range of I/Os, including cells for PCI/PC card applications. Each I/O cell occupies one I/O location and can be configured as an input, output or bidirectional, and has one pad associated with it. The output section of the I/O cell is configurable to one of four options: open drain, open source, tristate, or push-pull by suitable connection of the D and T inputs and each cell has a program pin that controls the slew rate of the output signal.

PACKAGING

- Wide range of surface mount and through board packages
- Various MQFP and ball grid array styles to international and JEDEC standards
- Ceramic equivalents to most plastic packages for fast prototyping
- Ongoing commitment to new package development

PACKAGING OPTIONS

The package style and pin count information is intended only as a guide. Detailed package specifications are available from Mitel Design Centres on request. New packages are being continually introduced, so if a particular package is not listed, please enquire through your Mitel sales representative.

The package dimensions implicit in the package `Code,' pitch and height dimensions are approximate and for guidance only. If detailed information is required, an outline drawing will be provided on request. All package dimensions are in mm.

A stock is held of the preferred packages to ensure a fast prototype assembly turn around. Alternative array size to package combinations are available, but not always stocked.

CLA90000 SERIES

Key to packages,

1234	=	Format number of preferred array/qualified package combination.
1234	=	Check availability with Mitel.
1234 ^	=	Check prototype package with Mitel.
†	=	In development.
1234 *	=	Maximum number of ceramic prototypes is 10 ONLY
1234 ^	=	NO footprint compatible ceramic prototypes are available

High Density Pad Array Production Packages

Metric Quad Flat Pack - Plastic

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
	44	MQFP44-GP-1010	0.80	2.0	1897	1897	1897	1897^	1897^	1897^	
	52	MQFP52-GP-1010	0.65	2.0	2155	2155	2155				
	64	MQFP64- GP-1420	1.00	2.8	1755	1755	1755	1755	1755	1755	1755
	64	MQFP64-GP-1414	0.80	2.0						2172	2172
M	64	MQFP64-GP-1414	0.80	2.8	1835	1835	1835	1835	1835		
Q	80	MQFP80-GP-1420	0.80	2.8	2157^	2157	2157	2157	2157	2157	2157
F	80	MQFP80-GQ-1414	0.65	2.0	1807	1808	1808	1808	1808	1808	1808
P	100	MQFP100-GP-1420	0.65	2.8	2166	2158	2158	2158	2158	2158	2158
	120	MQFP120-GP-2828	0.80	3.4	1730	1730	1899	1899	1899	1899	1899
	128	MQFP128-GP-2828	0.80	3.4	1752^	1752	2100	2100	2100	2100	2100
	144	MQFP144-GP-2828	0.65	3.4			2159^	2159	2159	2159	2159
	160	MQFP160-GP-2828	0.65	3.4				1882^	1882^	1882^	1882

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
	64	MQFP64-GP-1414	0.80	2.0	2172	2172					
M	64	MQFP64-GP-1414	0.80	2.8							
Q	80	MQFP80-GP-1420	0.80	2.8	1711	1711	1711^				
F	80	MQFP80-GQ-1414	0.65	2.0	1808	1808					
P	100	MQFP100-GP-1420	0.65	2.8	2158	2158					
	120	MQFP120-GP-2828	0.80	3.4	1899	1899	1899	1732	1732	1732	
	128	MQFP128-GP-2828	0.80	3.4	2100	2100	2100				
	144	MQFP144-GP-2828	0.65	3.4	2159	2159					
	160	MQFP160-GP-2828	0.65	3.4	1882	1882	1882	1882	1882	2118	2118^

FQFP (Fine pitch) - Plastic

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
F	100	FQFP100-FP-1414	0.50	2.0	1810	2156	2156	2156	2156	2156	2156
Q	208	FQFP208-FP-2828	0.50	3.4						2160^	2160^
F											
P											

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
F	100	FQFP100-FP-1414	0.50	2.0	2156	2156					
Q	208	FQFP208-FP-2828	0.50	3.4	2160^	2160^	2160	2160	2160	2160	
F	240	FQFP240-FP-3232	0.50	3.4	2163^	2163^	2163^	2163^	2163^	2163	2163
P	304	FQFP304-FP-4040	0.50	3.8					3030	3030	3030

LQFP (Low Profile) - Plastic

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
	48	LQFP48-FP-0707	0.50	1.4	2168^	2168^					
L	64	LQFP64-FP-1010	0.50	1.4	2130	2130	2130	2130 ^	2130 ^	2130 ^	
Q	80	LQFP80-GP-1414	0.65	1.4	1889	1889	1889	1889	1889		
F	100	LQFP100-FP-1414	0.50	1.4	1887	1887	1887	1888	1888	1888	1888
P	144	LQFP144-FP-2020	0.50	1.4	2164^	2164^	2164^	2164	2164	2164	2164
	176	LQFP176-FP-2424	0.50	1.4			2165^	2165^	2165^	2165^	2165

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
L											
Q	100	LQFP100-FP-1414	0.50	1.4	1888	1888					
F	144	LQFP144-FP-2020	0.50	1.4	2237	2237	2237	2237^			
P	176	LQFP176-FP-2424	0.50	1.4	2165	2165	2165				

CLA90000 SERIES

P2QFP ('PowerQuad 2') - Plastic with Copper Heat Slug

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
	100	P2QFP100-GH-1420	0.65	2.8				2202	2202	2202	2202
P	120	P2QFP120-GH-2828	0.80	3.4			3002	3002	3002	3002	3002
2	128	P2QFP128-GH-2828	0.80	3.4			2221	2221	2221	2221	2221
Q	144	P2QFP144-GH-2828	0.65	3.4				2222	2222	2222	2222
F	160	P2QFP160-GH-2828	0.65	3.4				2223	2223	2223	2223
P	208	P2QFP208-GH-2828	0.50	3.4							2225

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
	100	P2QFP100-GH-1420	0.65	2.8							
P	120	P2QFP120-GH-2828	0.80	3.4	3002	3002	2200	2200	2200	2200	2200^
2	128	P2QFP128-GH-2828	0.80	3.4	2221	2221	2221	2221	2221	2203	2203
Q	144	P2QFP144-GH-2828	0.65	3.4	2222	2222	2222	2222	2222	2226	2226^
F	160	P2QFP160-GH-2828	0.65	3.4	2223	2223	2223	2223	2223	2196	2196^
P	208	P2QFP208-GH-2828	0.50	3.4	2225	2225	2225	2225	2225	2225	2225
	240	P2QFP240-GH-3232	0.50	3.4	2228^	2228^	2228^	2228^	2228^	2228	2228
	304	P2QFP304-GH-4040	0.50	3.4					†	†	†

P4QFP ('PowerQuad 4') - Plastic with Copper Heat Slug

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
P	100	P4QFP100-GH-1420	0.65	2.8		2236	2236	2236	2236	2236	2236
4	120	P4QFP120-GH-2828	0.80	3.37			3005	3005	3005	3005	3005
Q	128	P4QFP128-GH-2828	0.80	3.42			3008	3008	3008	3008	3008
F	160	P4QFP160-GH-2828	0.65	3.37					3011	3011	3011
P	208	P4QFP208-GH-2828	0.50	3.49							3014

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
	100	P4QFP100-GH-1420	0.65	2.8	2236	2236					
P	120	P4QFP120-GH-2828	0.80	3.37	3006	3006	3006	3006	3006	3007	3007^
4	128	P4QFP128-GH-2828	0.80	3.42	3009	3009	3009	3010	3010	3010	3010
Q	160	P4QFP160-GH-2828	0.65	3.37	3011	3012	3012	3012	3012	3012	3013^
F	208	P4QFP208-GH-2828	0.50	3.49	3014	3014	3014	3014	3014	3015	3015
P	240	P4QFP240-GH-3232	0.50	3.4	3017^	3017^	3017^	3017^	3016^	3016	3016
	304	P4QFP304-GH-4040	0.50	3.8					3018^	3018^	3018^

BGA, Ball Grid Array - Plastic

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
P	169	PBGA169-BP-2323	1.50	2.09					†	†	†
B	225	PBGA225-BP-2727	1.50	2.09						†	†
G	313	PBGA313-BP-3535	2.54	2.29							
A	352	PBGA352-BP-3535	1.27	2.29							

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
P	169	PBGA169-BP-2323	1.50	2.09	†	†	†				
B	225	PBGA225-BP-2727	1.50	2.09	†	†	†	†	†	†	
G	313	PBGA313-BP-3535	2.54	2.29					†	†	†
A	352	PBGA352-BP-3535	1.27	2.29							†

TQFP (Thin Profile) - Plastic

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
	48	TQFP48-TP-0707	0.50	1.0	2117	2117					
T	64	TQFP64-TP-1010	0.50	1.0	†	†	†	†	†	†	
Q	80	TQFP80-TP-1414	0.50	1.0		†	†	†	†	†	
F	100	TQFP100-TP-1414	0.50	1.0			†	†	†	†	†
P	144	TQFP144-TP-2020	0.50	1.0				†	†	†	†

PLCC (Plastic J - Leaded Chip Carrier)

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
P	44	PLCC44-HP-1717	1.27	4.57	1491	1491	1491	1491	1491	1491	1491
L	68	PLCC68-HP-2525	1.27	5.08	1659	1659	1659	1659	1659		
C	84	PLCC84-HP-3030	1.27	5.08	1660	1660	1660	1660	1660	1660	1660
C											

CLA90000 SERIES

High Density Pad Array Prototyping Packages

Important: CQFP/CBGA packages are intended for prototyping only. Production capability is available in special cases.

Prototypes for MQFPs and P2 & P4 MQFPs

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
	44	CQFP44-GG-1010	0.80	3.2	1735*	1735*	1735*	†*	†	†	
	52	CQFP52-GG-1010	0.65	3.2	1800*	1800*	1800*				
	64	CQFP64- GG-1420	1.00	2.8	1773*	1773*	1773*	1773*	1773	1772	1772
C	64	CQFP64-GG-1414	0.80	2.8	2169*	2169*	2169*	2169*	2169	2169	2169
Q	80	CQFP80-GG-1420	0.80	2.8		1740*	1740*	1740*	1771	1771	1771
F	80	CQFP80-GG-1414	0.65	2.8	2102*	2102*	2102*	2102*	2102	1863	1863
P	100	CQFP100-GG-1420	0.65	2.8	1865*	1865*	1864*	1864*	1864	1864	1864
	120	CQFP120-GG-2828	0.80	3.6	1736*	1736*	1736*	1736*	1736	1737	1737
	128	CQFP128-GG-2828	0.80	3.6		1861*	1861*	1861*	1861	1861	1861
	144	CQFP144-GG-2828	0.65	3.6				1816*	1816	1816	1816
	160	CQFP160-GG-2828	0.65	3.6					1769	1769	1769

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
	64	CQFP64-GG-1414	0.80	2.8	2169	2169					
	80	CQFP80-GG-1420	0.80	2.8	1779	1779					
	80	CQFP80-GG-1414	0.65	2.8	1863	1863					
C	100	CQFP100-GG-1420	0.65	2.8	1864	1864					
Q	120	CQFP120-GG-2828	0.80	3.6	1737	1737	1737	1737	1737	1737	
F	128	CQFP128-GG-2828	0.80	3.6	1726	1726	1726	1726	1726	1726	1726
P	144	CQFP144-GG-2828	0.65	3.6	1816	1816	1816	1770	1770	1770	
	160	CQFP160-GG-2828	0.65	3.6	1769	1769	1769	1769	1769	1769	

Prototypes for FQFP, LQFP and P2 & P4 MQFPs

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
C	100	CQFP100-FG-1414	0.50	2.8	1860*	1860*	1860*	2101*	2101	2101	
Q	176	CQFP176-FG-2424	0.50	3.77					2217	2217	2217
F	208	CQFP208-FG-2828	0.50	3.6							2141
P											

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
C	100	CQFP100-FG-1414	0.50	2.8	2101	2101					
Q	176	CQFP176-FG-2424	0.50	3.77	2217	2217	2217	2217	2217	2217	
F	208	CQFP208-FG-2828	0.50	3.6	2141	2141	2141	2141	2141	2141	2141
P	240	CQFP240-FG-2828	0.50	3.6	2143	2143	2143	2143	2143	2143	2143

Prototypes for PLCC

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
C	44	CcLCC44-HC-1717	1.27	3.43	1716	1716	1716	1716	1716	1716*	1716*
c	68	CcLCC68-HC-2525	1.27	3.43	1621	1621	1621	1621	1621		
L	84	CcLCC84-HC-3030	1.27	3.43	1626	1626	1626	1626	1626	1473*	1473*
C											
C											

Prototypes for BGAs

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
C	169	CBGA169-BC-2323	1.50	2.09					†	†	†
B	225	CBGA225-BC-2727	1.50	2.09						†	†
G	313	CBGA313-BC-3535	2.54	2.29							
A	352	CBGA352-BC-3535	1.27	2.29							

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
C	169	CBGA169-BC-2323	1.50	2.09	†	†	†				
B	225	CBGA225-BC-2727	1.50	2.09	†	†	†	†	†	†	
G	313	CBGA313-BC-3535	2.54	2.29					†	†	†
A	352	CBGA352-BC-3535	1.27	2.29							†

Prototypes for TQFPs

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
C	64	CQFP64-FG-1010	0.50	3.2	2103*	2103*	2103*	†*	†	†	
Q	80	CQFP80-GG-1414	0.65	2.8	2102*	2102*	2102*	2102*	2102	1863	1863
F	100	CQFP100-FG-1414	0.50	2.8	1860*	1860*	1860*	2101*	2101	2101	
P	144	CQFP144-FG-2020	0.50	3.6				2104	2104	2104	

CLA90000 SERIES

Standard Density Pad Array Packages, Military Arrays

LdCC

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
L	132	LdCC132-GCA-2424	0.64	2.57	1840	1840	1840	1840	1840	1840	1662
d	172	LdCC172-GCA-3030	0.64	2.82						1668	1668
C	196	LdCC196-GCA-3535	0.64	2.82						1672	1672
C											

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
L	132	LdCC132-GCA-2424	0.64	2.57	1662	1662	1662	1662	1662		
d	172	LdCC172-GCA-3030	0.64	2.82	1668	1668	1668	1668	1668	1669	1669
C	196	LdCC196-GCA-3535	0.64	2.82	1672	1672	1672	1672	1672	1672	1831
C											

LdCC & TLdCC - Power

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
L	132	LdCC132-GCP-2424	0.64	3.33							1841
d	172	LdCC172-GCP-3030	0.64	3.58							1836
C	196	LdCC196-GCP-3535	0.64	3.58						1839	1839
C	256	LdCC256-GCP-3737	0.51	3.66							
T	132	TLdCC132-YCP-2424	0.62	3.3							
L	172	TLdCC172-YCP-3030	0.62	3.56							
d	320	TLdCC320-YCP-4444	0.5	2.64							

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
L	132	LdCC132-GCP-2424	0.64	3.33	1841	1841	1841	1841	1841		
d	172	LdCC172-GCP-3030	0.64	3.58	1836	1836	1836	1836	1836	1762	1762
C	196	LdCC196-GCP-3535	0.64	3.58	1839	1839	1839	1839	1839	1839	1739
C	256	LdCC256-GCP-3737	0.51	3.66			1834	1834	1834	1834	1834
T	132	TLdCC132-YCP-2424	0.62	3.3		3023	3023	3023	3023	3025	3025
L	172	TLdCC172-YCP-3030	0.62	3.56						3027	3027
d	320	TLdCC320-YCP-4444	0.5	2.64		2206	2206	2206	2206	2206	2206

PGA

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
	68	PGA68-ACA-2828	2.54	4.14	1462	1462	1462	1462	1462	1463	1463
	84	PGA84-ACA-2828	2.54	4.14	1479	1479	1479	1479	1479		
P	100	PGA100-ACA-3434	2.54	4.14			1480	1480	1480	1480	1480
G	120	PGA120-ACA-3434	2.54	4.14			1481	1481	1481	1481	1481
A	132	PGA132-ACA-3636	2.54	4.14				1467	1467	1467	1467
	144	PGA144-ACA-4040	2.54	4.14							1468
	180	PGA180-ACA-4040	2.54	4.14						1484	1484
	181	PGA181-ACA-4040	2.54	4.14							2216
	257	PGA257-ACA-5151	2.54	4.14							

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
	100	PGA100-ACA-3434	2.54	4.14	1480	1465	1465	1465			
	120	PGA120-ACA-3434	2.54	4.14	1481	1466	1466	1466			
P	132	PGA132-ACA-3636	2.54	4.14	1467	1467	1467				
G	144	PGA144-ACA-4040	2.54	4.14	1468	1468	1468	1468	1468	1468	
A	180	PGA180-ACA-4040	2.54	4.14	1484	1484	1484	1484	1484	1469	
	181	PGA181-ACA-4040	2.54	4.14	2216	2216	2216	2216	2216	2216	1844
	257	PGA257-ACA-5151	2.54	4.14			1824	1824	1824	1824	1824

PGA, Power

Style	Leads	Code	Pitch	Height	901	902	903	904	905	906	907
P	84	PGA(P)84-ACB-2828	2.54	6.15					†	†	1815
G	144	PGA(P)144-ACB-4040	2.54	6.15	2151	2151	2151	2151	2151	2151	2151
A	208	PGA(P)208-ACB-4545	2.54	4.45							
(P)	209	PGA(P)209-ACB-4545	2.54	4.45						1811	1811

Style	Leads	Code	Pitch	Height	908	909	910	911	912	913	914
P	84	PGA(P)84-ACB-2828	2.54	6.15	1815	1815	1815	1815	1815	1815	
G	144	PGA(P)144-ACB-4040	2.54	6.15	1812	1812	1812	1812	1812	1693	1693
A	208	PGA(P)208-ACB-4545	2.54	4.45			1838	1838	1838	1838	1838
(P)	209	PGA(P)209-ACB-4545	2.54	4.45	1811	1811	1811	1811	1811		

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